Docket No.: 394-1597 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	**OFFICIAL DRAFTSMAN**
	BATCH NO. Q42
Seiji SAWADA et al.	
Serial No. 08/246,582	Group Art Unit: 2511
	Allowed: October 26, 1995
Filed: May 19, 1994	Examiner: A. Zarabian

For: TEST CIRCUIT IN CLOCK SYNCHRONOUS SEMICONDUCTOR MEMORY DEVICE

LETTER SUBMITTING FORMAL DRAWINGS

Honorable Commissioner of
Patents and Trademarks
Washington, D. C. 20231

Sir:

In response to the Notice of Allowability dated October 26, 1995, submitted herewith are twenty-nine (29) sheets of Formal Drawing in connection with the above referenced application.

Respectfully submitted,

LOWE, PRICE, LEBLANC & BECKER

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enclosure
Date: December 22, 1995